```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity LetterImplementation is
 Port ( input_signal : in STD_LOGIC_VECTOR (7 downto 0);
 output_letter : out STD_LOGIC_VECTOR (7 downto 0));
end LetterImplementation;
architecture Behavioral of LetterImplementation is
begin
 process(input_signal)
 begin
 case input_signal is
 when "00000000" => output_letter <= "01000001"; -- 'A'
 when "00000001" => output_letter <= "01000010"; -- 'B'
 when "00000010" => output_letter <= "01000011"; -- 'C'
 when others => output_letter <= "00111111"; -- '?' for undefined input
 end case;
 end process;
end Behavioral;
```